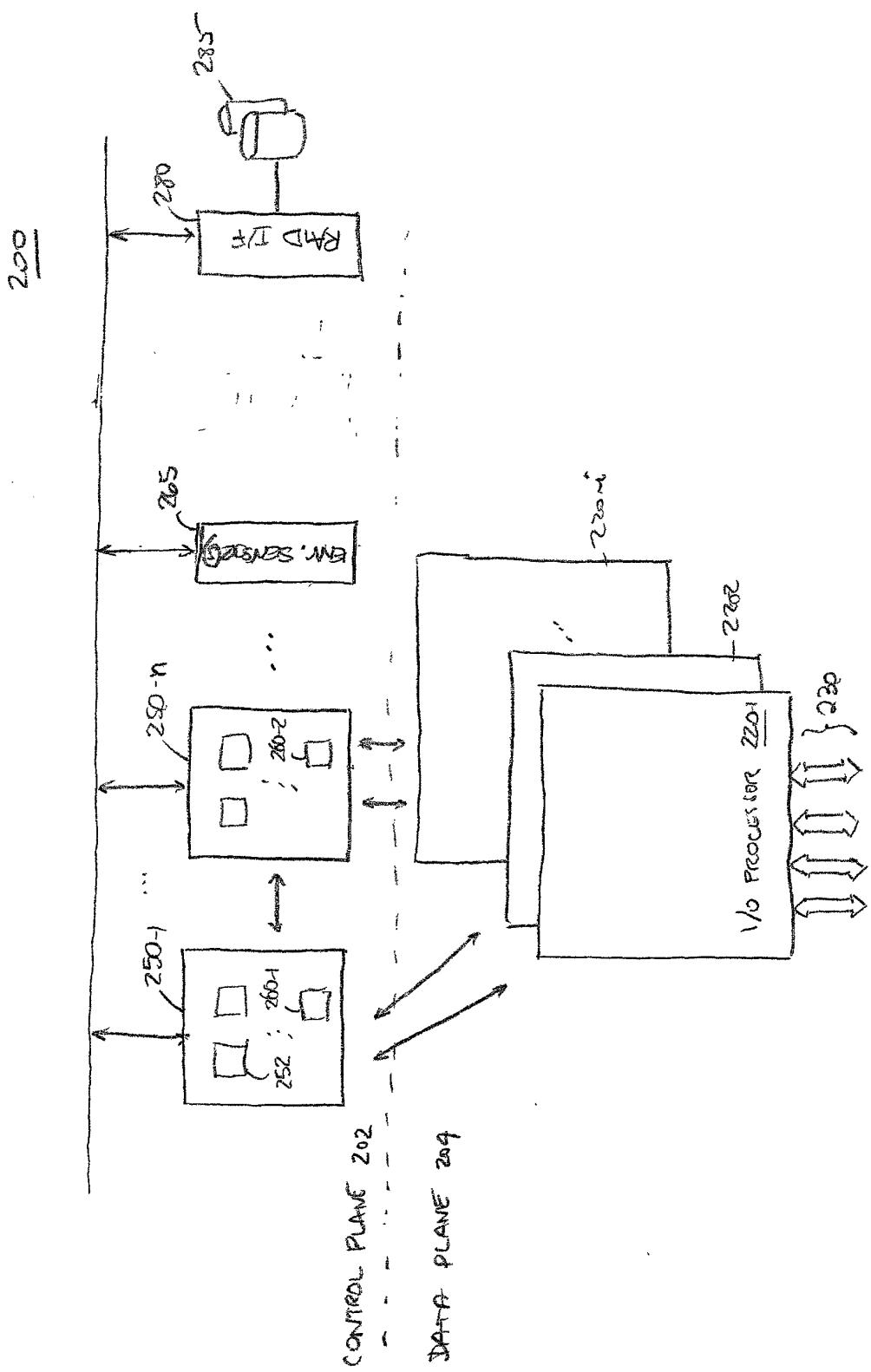


FIG. 1

FIG. 2



102,103

00000000000000000000000000000000

200

285

280

285

280-n

250-1

250-2

250-3

CONTROL PLANE 202

DATA PLANE 204

280

282

2201

I/O Processor 2201

2202

2203

2204

2205

2206

2207

2208

2209

22010

22011

22012

22013

22014

22015

22016

22017

22018

22019

22020

22021

22022

22023

22024

22025

22026

22027

22028

22029

22030

22031

22032

22033

22034

22035

22036

22037

22038

22039

22040

22041

22042

22043

22044

22045

22046

22047

22048

22049

22050

22051

22052

22053

22054

22055

22056

22057

22058

22059

22060

22061

22062

22063

22064

22065

22066

22067

22068

22069

22070

22071

22072

22073

22074

22075

22076

22077

22078

22079

22080

22081

22082

22083

22084

22085

22086

22087

22088

22089

22090

22091

22092

22093

22094

22095

22096

22097

22098

22099

220100

220101

220102

220103

220104

220105

220106

220107

220108

220109

220110

220111

220112

220113

220114

220115

220116

220117

220118

220119

220120

220121

220122

220123

220124

220125

220126

220127

220128

220129

220130

220131

220132

220133

220134

220135

220136

220137

220138

220139

220140

220141

220142

220143

220144

220145

220146

220147

220148

220149

220150

220151

220152

220153

220154

220155

220156

220157

220158

220159

220160

220161

220162

220163

220164

220165

220166

220167

220168

220169

220170

220171

220172

220173

220174

220175

220176

220177

220178

220179

220180

220181

220182

220183

220184

220185

220186

220187

220188

220189

220190

220191

220192

220193

220194

220195

220196

220197

220198

220199

220200

220201

220202

220203

220204

220205

220206

220207

220208

220209

220210

220211

220212

220213

220214

220215

220216

220217

220218

220219

220220

220221

220222

220223

220224

220225

220226

220227

220228

220229

220230

220231

220232

220233

220234

220235

220236

220237

220238

220239

220240

220241

220242

220243

220244

220245

220246

220247

220248

220249

220250

220251

220252

220253

220254

220255

220256

220257

220258

220259

220260

220261

220262

220263

220264

220265

System Card Interconnect

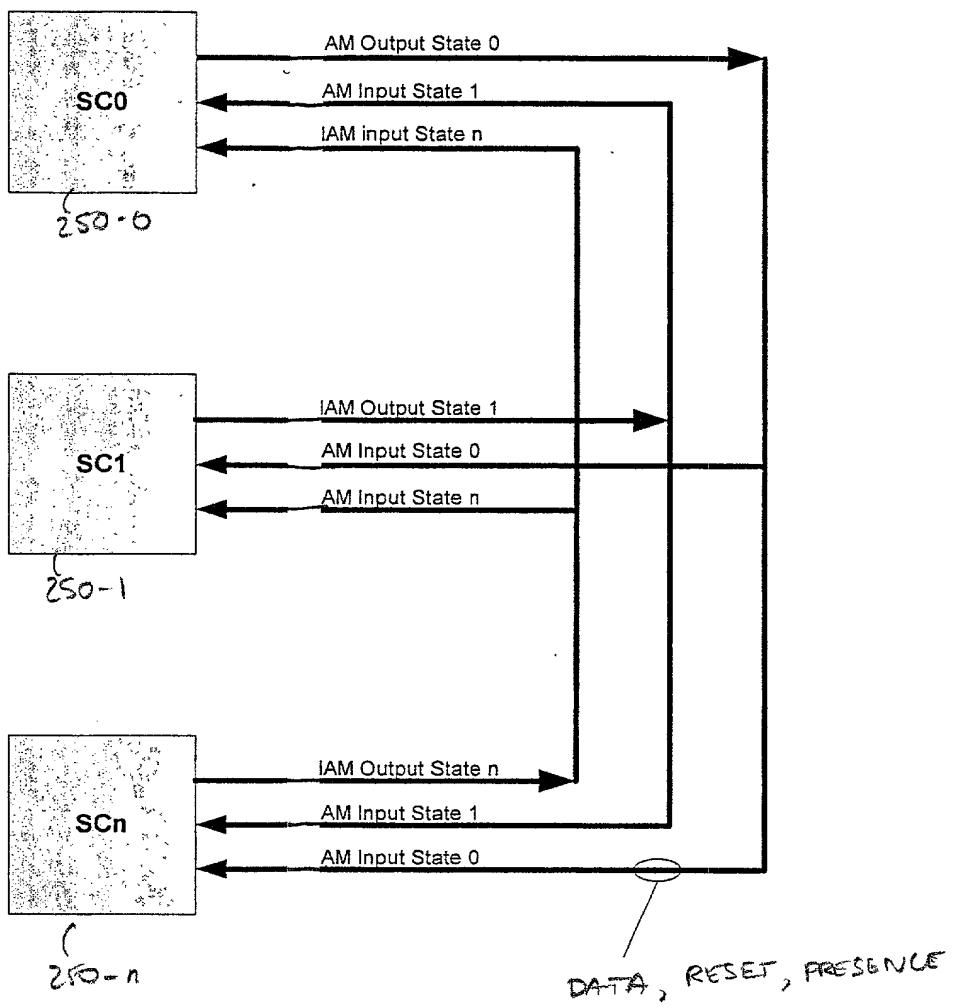


FIG. 3

Transitions

$I \Rightarrow P$ (more than one cpu card is present)
 $I \Rightarrow C$ (only one cpu card is present)
 $P \Rightarrow C$ (the Pause State duration expired)
 $C \Rightarrow I$ (temporary/committed identity conflict encountered)
 $C \Rightarrow W$ (identity committed to master-write register)
 $W \Rightarrow W$ (wait for event)

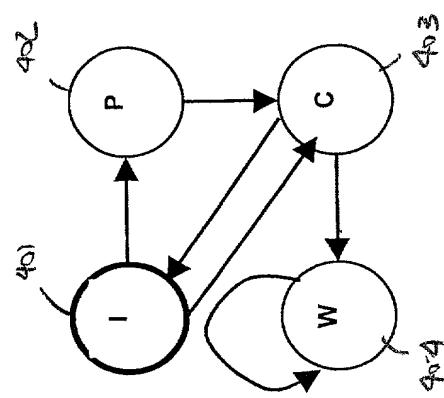


FIG. 4

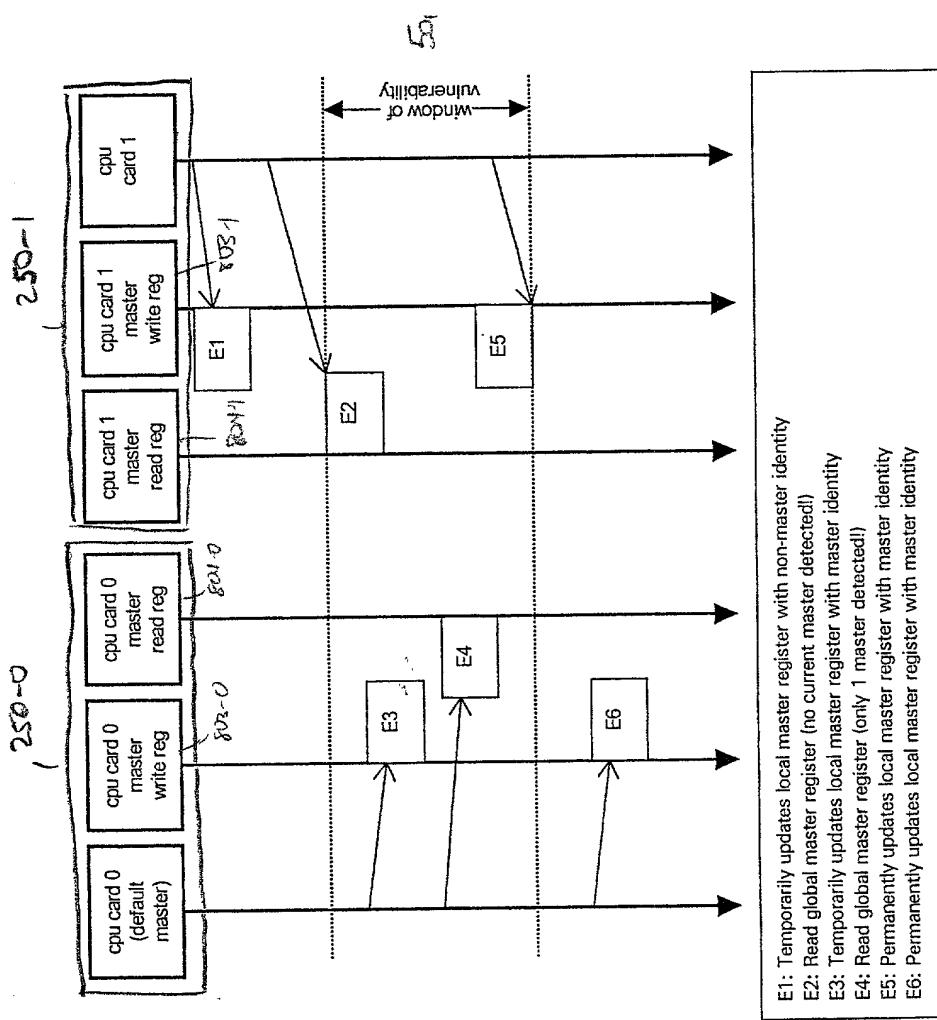


FIG. 5

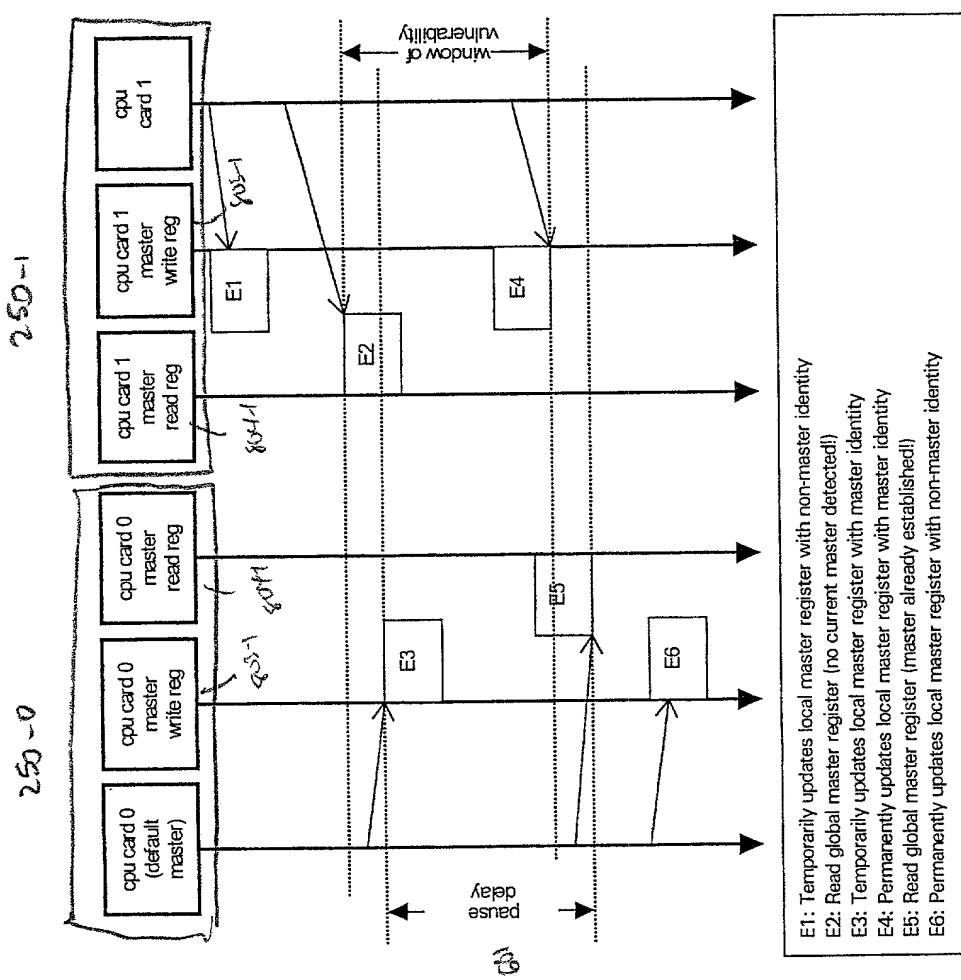


FIG. 6

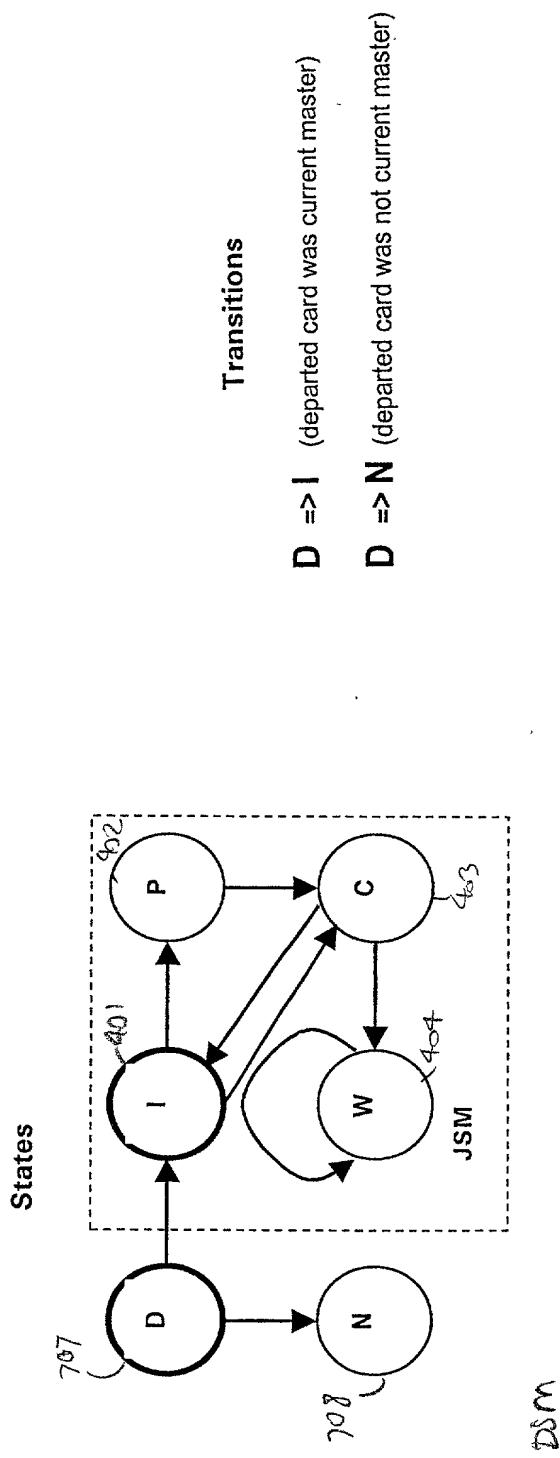


FIG. 7

Bit field	R/W	Default	Function
0	R/W	0	SC Master state
31:2	R/w	0x0000000	Reserved

SC Master Register

FIG. 8A

Bit field	R/W	Default	Function
0	R	0	SC0 present
1	R	0	SC1 present
n	R	0	SCn present
31:n+1	R	0x0000000	Reserved

SC Slot Presence Register

FIG. 8B

Bit field	Host R/W	Default	Function
7:0	R/w	0x00	Software specified
31:8	R	0x0000000	Reserved

AM Master Write Register

FIG. 8C

Bit field	Host R/W	Default	Function
7:0	R	0x00	RSC .. AM state (software specified)
31:8	R	0x0000000	Reserved

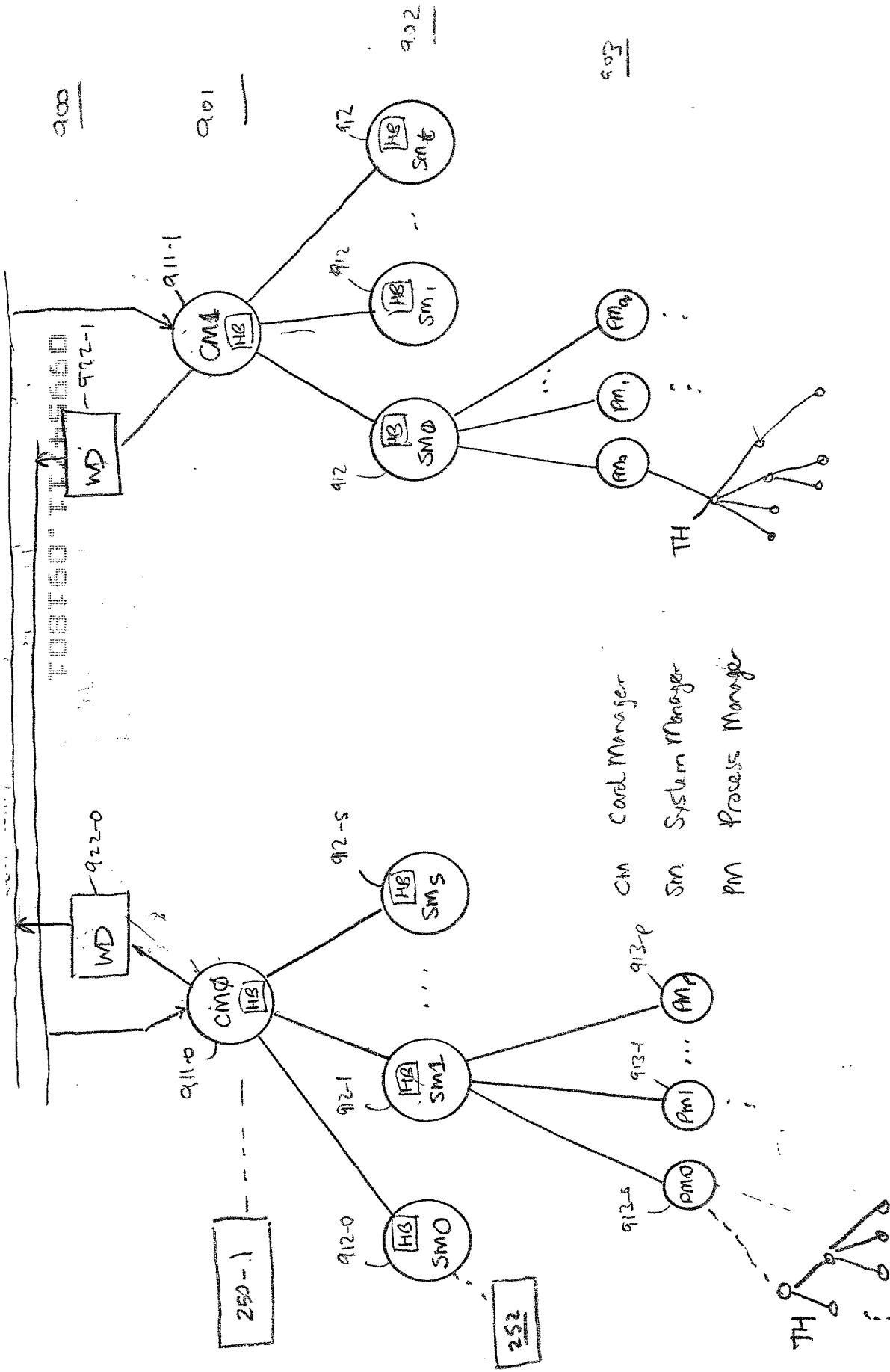
AM Master Read Register

FIG. 8D

Bit field	Host R/W	Default	Function
0	W/R	0x0	AM Receive Data Interrupt
1	R	0x00000	AM Reset Interrupt (RSC has been reset)
2	R	0x00000	AM Slot Change Interrupt (RSC inserted or extracted)
31:8	R	0x0000000	Reserved

AM Interrupt Status Register

FIG. 8E



Availability Manager (Am)
Software Hierarchy

FIG. 9

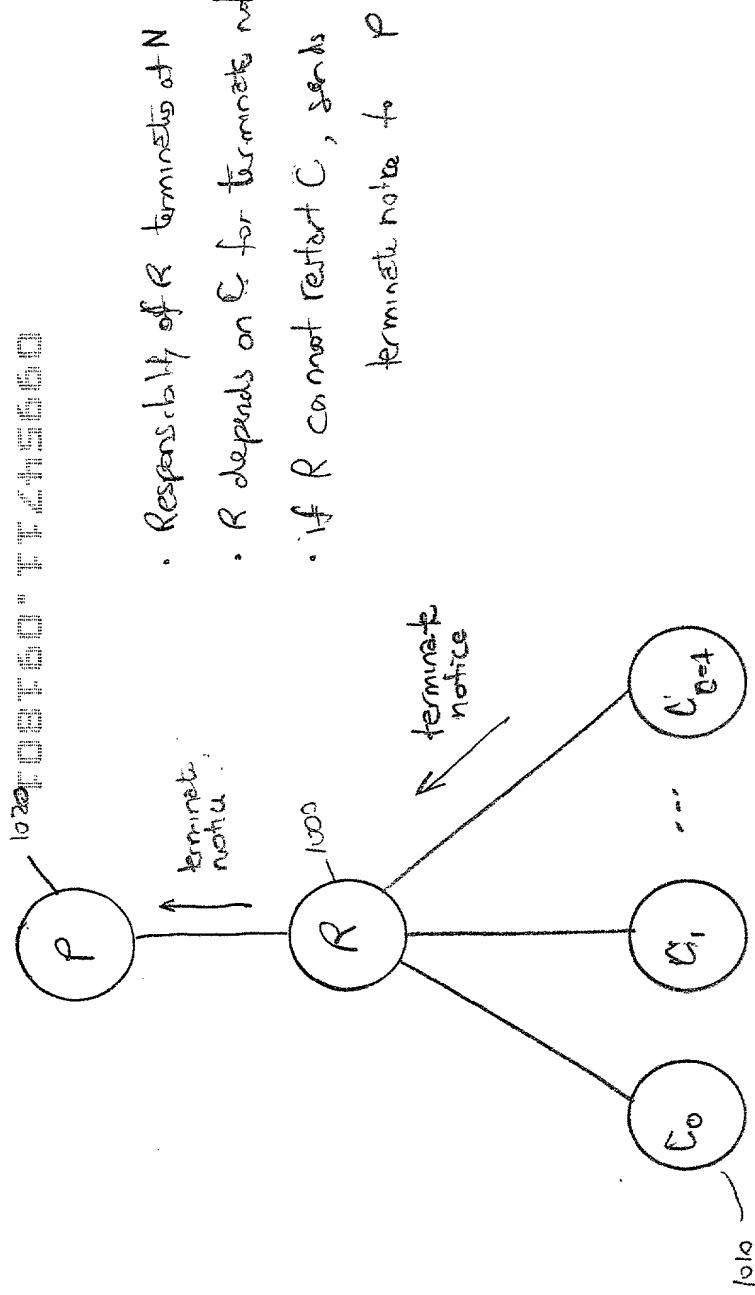


FIG. 10

$$R = CM, SM, PM$$

$$C = SM, PM, TH$$

$$P = WD, CM, SM$$

$R_n = CM, SM$

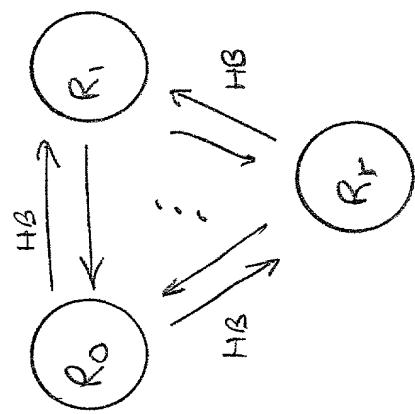


FIG. 11

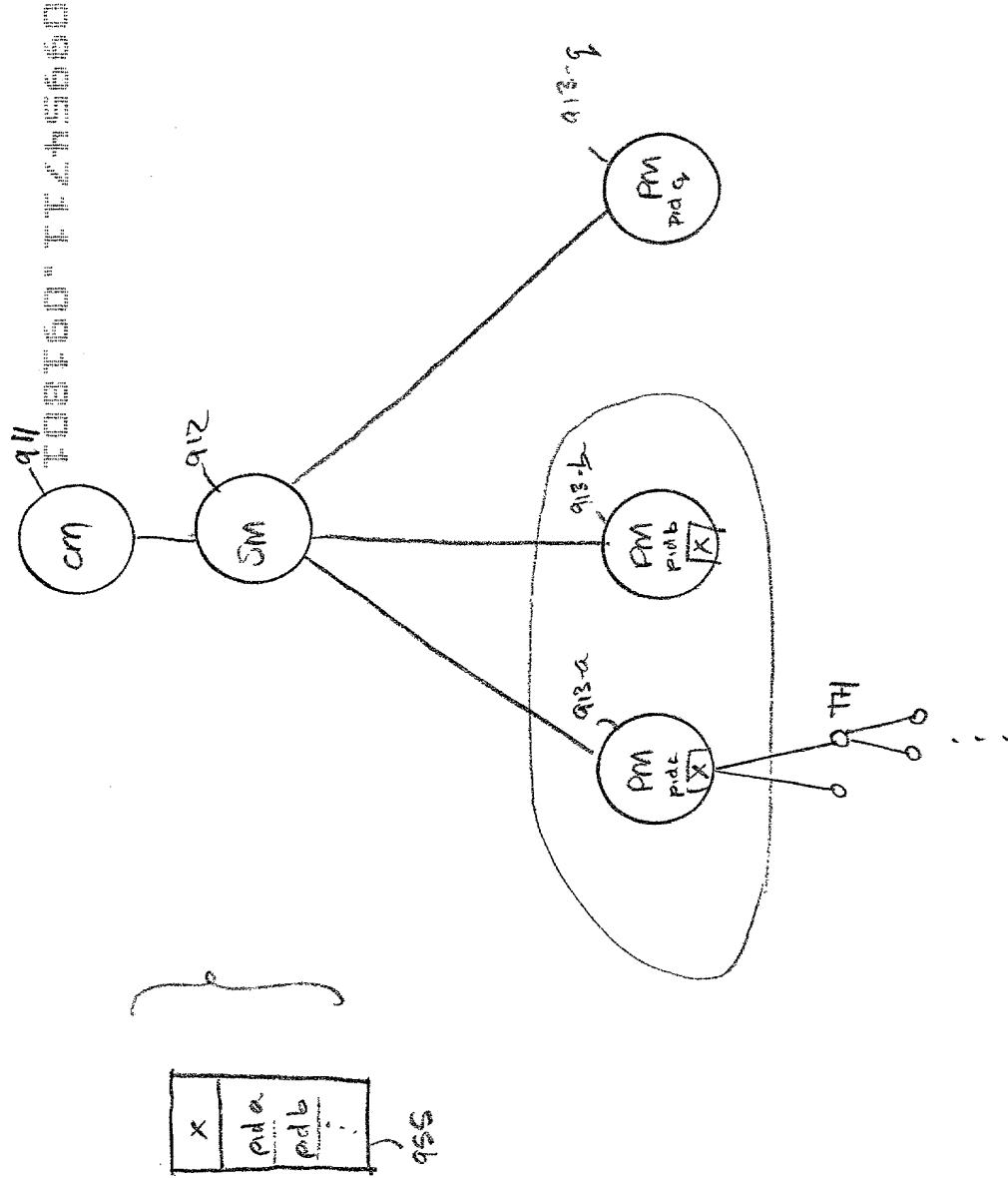


FIG. 12